Noise and Reliability in Advanced Bipolar Technologies

Md Mazhar Ul Hoque

Advisor: Prof. Zeynep Celik-Butler

Department of Electrical Engineering University of Texas at Arlington

Outline

- Introduction:
 - Limitations in existing noise models.
 - Importance and motivation of research.
- Noise in polysilicon emitter bipolar transistors:
 - Experimental setup.
 - S_{IB} modeling:
 - noise mechanisms, effect of bias, geometry and IFO.
 - S_{IC} modeling:
 - noise mechanisms, effect of bias and IFO.
 - S_{vr} modeling:
 - Collector-emitter measurement setup, effect of bias and IFO.
 - Computer codes.
- Noise in SiGe heterojunction bipolar transistors:
 - Dominant noise source.
 - Effect of selective collector implant.
 - Effect of higher extrinsic base implant.
 - Effect of SiGe epi-SiGe poly interface.
 - Effect of emitter-poly overlap.
 - Physical origin and modeling of S_{IB.}
- Conclusion

Current BJT low-frequency noise models

- **Gummel-Poon:** $I_{BN}^2 = \frac{KF \cdot I_B^{AF}}{f^{EF}} \cdot \Delta f$
- VBIC Flicker noise due to IBE, IBEP

• **MEXTRAM:**
$$\overline{iN_B^2} = \frac{MULT}{f} \left[KFN \left(\frac{|I_{B2}|}{MULT} \right)^2 + KF \left(\frac{|I_{B1}|}{MULT} \right)^2 \right] \cdot \Delta f$$

• MODELLA:
$$\overline{iN_B^2} = \frac{KF \cdot MULT^{1-AF} |I_{RE} + I_{LE}|^{AF}}{f} \cdot \Delta f$$

Importance and motivation

Limitations in existing noise models:

- Only one single noise source in base current: S_{IB}=KF.I_B^{AF}.
 - Noise in base current dominant only for higher base series resistance.
 - Does not include any geometry, temperature or process parameter.
- Noise in collector current and internal resistances are neglected.
 - Noise in collector current contributes at lower base series resistance.
 - Noise from internal resistance contributes at higher bias current.

Research goal:

- To model all possible noise sources in advanced bipolar transistors:
 - Noise in base current, collector current and internal resistances.
- Developing physics based scalable equations for the noise sources:
 - Incorporating geometry, temperature and process dependant parameters.
- Writing computer source code for device and circuit analysis CAD tools to incorporate all possible noise sources in BJT.

Advanced bipolar technologies under investigation

- Polysilicon emitter bipolar transistors:
 - 2nd generation BiCMOS technology, Texas Instruments Inc.
 - NPN and PNP transistors.
 - Variable size, variable IFO thickness.
- SiGe heterojunction bipolar transistors:
 - 1st generation BiCMOS technology, National Semiconductor Corporation.
 - NPN transistors.
 - Variable size, variable design rules.
 - Variable doping in base and collector.

Outline

- Introduction:
 - Limitations in existing noise models.
 - Importance and motivation of research.
- Noise in polysilicon emitter bipolar transistors:
 - Experimental setup.
 - S_{IB} modeling:
 - noise mechanisms, effect of bias, geometry and IFO.
 - S_{IC} modeling:
 - noise mechanisms, effect of bias and IFO.
 - S_{vr} modeling:
 - Collector-emitter measurement setup, effect of bias and IFO.
 - Computer codes.
- Noise in SiGe heterojunction bipolar transistors:
 - Dominant noise source.
 - Effect of selective collector implant.
 - Effect of higher extrinsic base implant.
 - Effect of SiGe epi-SiGe poly interface.
 - Effect of emitter-poly overlap.
 - Physical origin and modeling of S_{IB.}
- Conclusion

Collector-base measurement setup



UTA Noise and Reliability Laboratory

Collector-base measurement

$$S_{V_C} = x \cdot S_{V_r} + y \cdot S_{I_B} + z \cdot S_{I_C}$$
$$S_{V_B} = u \cdot S_{V_r} + v \cdot S_{I_B} + w \cdot S_{I_C}$$



$$S_{V_r} = S_{V_{r_e}} + S_{V_{r_b}}$$

for unity coherence:

If
$$S_{V_r}$$
 has the dominant contribution, $\frac{S_{V_C}}{S_{V_P}} \approx \frac{x}{u}$

If
$$S_{I_B}$$
 has the dominant contribution, $\frac{S_{V_A}}{S_V}$

$$\frac{S_{V_C}}{S_{V_B}} \approx \frac{y}{v}$$

U

If
$$S_{I_C}$$
 has the dominant contribution, $\frac{S_{V_C}}{S_{V_R}} \approx \frac{z}{N}$

Dominant noise source



 Calculated S_{VC}/S_{VB} considering S_{IB} contribution dominant closely matches experimental S_{VC}/S_{VB}; SIB contribution dominant.

Outline

- Introduction:
 - Limitations in existing noise models.
 - Importance and motivation of research.

Noise in polysilicon emitter bipolar transistors:

- Experimental setup.
- S_{IB} modeling:

noise mechanisms, effect of bias, geometry and IFO.

- S_{IC} modeling:
 - noise mechanisms, effect of bias and IFO.
- S_{vr} modeling:
 - Collector-emitter measurement setup, effect of bias and IFO.
- Computer codes.
- Noise in SiGe heterojunction bipolar transistors:
 - Dominant noise source.
 - Effect of selective collector implant.
 - Effect of higher extrinsic base implant.
 - Effect of SiGe epi-SiGe poly interface.
 - Effect of emitter-poly overlap.
 - Physical origin and modeling of S_{IB.}
- Conclusion

Area dependence of S_{IB} in NPN transistors



Internal emitter resistance and ideality factor of base current

1.6 1.5 1.4 ~ m = 27.8 g_{mi} + 1.07 1.3 Ξ r_e=27.8 ohm 1.2 n_b=1.07 1.1 1 1.0E-03 5.0E-03 9.0E-03 1.3E-02 1.7E-02 g_{mi} (ohm⁻¹)

0.7x100 μ m² NPN, thickest IFO, R_S=1M Ω



Physical origin of S_{IB}

Base current dependence

 $S_{I_{B_{diff}}} \propto I_{B_{diff}}$

 $S_{I_{B_{rec}}} \propto I_{B_{rec}}^2$

diffusion fluctuation in emitter.

 $S_{I_{B_{tun}}} \propto I_{B_{tun}}^2$ tunneling fluctuation in IFO.

recombination fluctuation in emitter-base space charge region.

recombination fluctuation at spacer oxide interface.

- Emitter perimeter dependence
 - Noise source distributed homogeneously around the emitter.
 - Recombination fluctuation at the spacer oxide interface.
- Emitter area dependence
 - Noise source distributed homogeneously underneath the emitter.
 - Diffusion fluctuation in emitter or tunneling fluctuation in IFO.

Physical origin of S_{IB} (cont.)

$$S_{I_B} = S_{I_{B_{diff}}} + S_{I_{B_{tun}}} + S_{I_{B_{rec}}}$$

• Unity ideality factor of I_B megligible $I_{B_{rec}}$. negligible $S_{I_{B_{rec}}}$.

$$S_{I_B} \approx S_{I_{B_{diff}}} + S_{I_{B_{tun}}}$$

Diffusion and tunneling fluctuation component of S_{IB}

0.7x100 μ m² NPN, medium IFO, R_s=1M Ω



Area dependence of tunneling fluctuation of S_{IB} in PNP transistors



Tunneling-fluctuation source homogeneously distributed underneath the emitter.

Smaller device-dimension severely affected by lateral diffusion and mask undercut; effective emitter area considered.

Diffusion fluctuation in S_{IB}

$$\frac{S_{I_{B_D}}}{I_B} = \frac{\frac{\alpha_m q}{D_m f} \ln\left[\frac{p(0)}{p(x_1)}\right] + \frac{\alpha_p q}{D_p f} \ln\left[\frac{p(x_2)}{p(x_3)}\right]}{\left(\frac{W_m}{D_m} + \frac{W_p}{D_p} + \frac{1}{s_{ox}} + \frac{1}{s_m}\right)^2}$$

$$\alpha_m$$
 : Hooge parameter in mono-Si
 α_p : Hooge parameter in poly-Si
Assumption: $\alpha_m = \alpha_p = \alpha$

$$\boxed{\frac{p(x_2)}{p(x_3)} \approx 1 + \frac{s_m W_p}{D_p}}$$

$$\frac{p(0)}{p(x_1)} = 1 + \frac{W_m}{D_m} \left(\frac{1}{s_{ox}} + \frac{1}{s_m} + \frac{W_p}{D_p}\right)^{-1}$$



Tunneling fluctuation in S_{IB}

$$\frac{S_{I_{B_T}}}{I_B^2} = \left[1 + s_{ox} \left(\frac{1}{s_m} + \frac{W_m}{D_m} + \frac{W_p}{D_p}\right)\right]^{-2} \frac{S_{t_{mn}}}{t_{mn}^2}$$

- *t_{mn}* **tunneling probability of minority carriers**
- $S_{t_{mn}}$ fluctuation in t_{mn}
- *m*^{*} effective mass of minority carriers
- *q* electronic charge
- *k* Boltzmann constant
- *L* **IFO thickness**

$$\frac{S_{t_{mn}}}{t_{mn}^2} = \frac{m^* q k T L^3 \tan \delta}{3 V_o \hbar^2 \pi \varepsilon_{ox} A f}$$

- *V_o* barrier height for the minority carriers
- *ħ* modified Planck's constant
- *A* area of IFO
- $\tan \delta$ loss tangent of the oxide

Scaling effect on S_{IB}

AF for S_{IB} in PNP transistors

Relative	AF		
	0.7x100	0.7x0.7	
IFO thickness	(µm²)	(µm²)	
thickest	1.12	1.89	
medium	1.23	2.09	
thinnest	1.01		

$$S_{I_B} = KF \cdot I_B^{AF}$$

$$S_{I_B} \approx S_{I_{B_{diff}}} + S_{I_{B_{tun}}}$$
$$= KF_D \cdot I_B + KF_T \cdot I_B^2$$

- Diffusion fluctuation dominant in large (0.7x100µm²) devices.
- Tunneling fluctuation dominant in small (0.7x0.7µm²) devices.

Scaling effect on S_{IB} in PNP transistors with thickest IFO



UTA Noise and Reliability Laboratory



- Thicker polysilicon in smaller transistors.
- Lower dopant concentration; shallower junction.
 - higher chance for minority carriers from base to reach and tunnel through the oxide interface; tunneling fluctuation dominant.
 - FLUORINE EFFECT: fluorine enhances oxide break-up.
 - lower fluorine (from BF₂) concentration causes less oxide breakup in smaller PNP devices; increased tunneling: (no fluorine in the transistors studied here)



- Polysilicon surface almost perpendicular to wafer surface at emitter window sidewall.
- Reduced doping concentration in the perimeter region.
- Shallower junction close to emitter window perimeter.
- An overlap of the emitter-base space charge region with poly-mono silicon interface might occur close to perimeter.

Perimeter depletion effect in smaller transistors



- For smaller transistors
 - perimeter/area ratio increases sharply.
 - non ideal peripheral component of base current increases.
 - fluctuation in non-ideal base current might become significant.

Effect of IFO on DC characteristics of 0.7x100µm² NPN transistors



IFO increases the current gain significantly.

Effect of IFO on DC characteristics of 0.7x100µm² PNP transistors



 No significant improvement in current gain with increasing IFO thickness.

Effect of interfacial oxide on S_{IB} in NPN and PNP transistors



IFO increases S_{IB} both in NPN and PNP transistors.

Difference in the effect of IFO in NPN and PNP transistors

0.7x100µm² transistors

Device type	AF	
PNP	~ 1	
NPN	~ 1.5	

$$S_{I_B} = KF \cdot I_B^{AF}$$

$$S_{I_B} \approx S_{IB_{diff}} + S_{IB_{tun}}$$
$$= KF_D \cdot IB + KF_T \cdot IB^2$$

- In PNP, diffusion fluctuation in mono and poly-silicon emitter dominates; less effect of IFO.
- In NPN, both diffusion fluctuation in mono and polysilicon emitter, and tunneling fluctuation through IFO contribute.

Physics behind difference in NPN and PNP transistors

- Hole barrier height larger than electron barrier height at interfacial oxide:
 - minority carriers (holes) severely suppressed in NPN; significant current gain improvement.
 - minority carriers (electrons) not suppressed significantly in PNP; little current gain improvement.
- Effect of fluorine:
 - fluorine accelerates oxide break-up.
 - fluorine from emitter dopant BF₂ in PNP creates more oxide breakup; reduced tunneling and increased diffusion through broken oxide.
- Increased oxide breakup and faster diffusion of boron makes the emitter deeper in PNP:
 - increased recombination-base current, reduced current gain improvement.
 - higher diffusion fluctuation in larger monosilicon emitter region.
- Different oxidation rate of the base material could create different IFO thickness for NPN and PNP transistors on the same wafer.

Outline

- Introduction:
 - Limitations in existing noise models.
 - Importance and motivation of research.

• Noise in polysilicon emitter bipolar transistors:

- Experimental setup.
- S_{IB} modeling:
 - noise mechanisms, effect of bias, geometry and IFO.
- S_{IC} modeling:

noise mechanisms, effect of bias and IFO.

- S_{vr} modeling:
 - Collector-emitter measurement setup, effect of bias and IFO.
- Computer codes.
- Noise in SiGe heterojunction bipolar transistors:
 - Dominant noise source.
 - Effect of selective collector implant.
 - Effect of higher extrinsic base implant.
 - Effect of SiGe epi-SiGe poly interface.
 - Effect of emitter-poly overlap.
 - Physical origin and modeling of S_{IB.}
- Conclusion

Effect of interfacial oxide on S_{IC}



IFO increases S_{IC} both in NPN and PNP transistors.

S_{IC} modeling

$$S_{I_C} = S_{I_{C_N}} + S_{I_{C_D}}$$
$$= KF_N \cdot I_C^2 + KF_D \cdot I_C$$

Some researchers assign the same

origin of S_{IB} to S_{IC} .

$$S_{I_C} = \frac{S_{V_C}}{R_L^2}$$
 is merely an amplified S_{IB}.



Number fluctuation in S_{IC} requires further investigation.

Diffusion fluctuation in S_{IC}

$$\frac{S_{I_{C_D}}}{I_C} = \frac{qD\alpha}{W_B^2 f} \ln\left(\frac{n(0)}{n(W_B)}\right)$$

$$\frac{n(0)}{n(W_B)} \approx \frac{\upsilon_s + D/W_B}{D/W_B}$$

$$\upsilon_s \quad \text{saturated drift velocity}$$



Outline

- Introduction:
 - Limitations in existing noise models.
 - Importance and motivation of research.

• Noise in polysilicon emitter bipolar transistors:

- Experimental setup.
- S_{IB} modeling:
 - noise mechanisms, effect of bias, geometry and IFO.
- S_{IC} modeling:
 - noise mechanisms, effect of bias and IFO.
- S_{vr} modeling:

Collector-emitter measurement setup, effect of bias and IFO.

- Computer codes.
- Noise in SiGe heterojunction bipolar transistors:
 - Dominant noise source.
 - Effect of selective collector implant.
 - Effect of higher extrinsic base implant.
 - Effect of SiGe epi-SiGe poly interface.
 - Effect of emitter-poly overlap.
 - Physical origin and modeling of S_{IB.}
- Conclusion

Effect of bias on coherence in NPN and PNP transistors



Coherence decreases with increasing bias in NPN transistor.

Effect of varying base bias resistance (R_S) on S_V

0.7x100 µm² NPN, thickest IFO, IB=384nA



- S_{vc} does not decrease any more for R_s smaller than 1 k Ω .
- S_{VB} becomes comparable to system background noise for R_S smaller than 10 kΩ.

Collector-emitter measurement setup



Dominant noise source in collector-emitter measurement



S_{IC} in collector-emitter measurement

thickest IFO : AFC=3.21 **10⁻¹⁴** medium IFO : AFC=3.58 S_{IC} (A²/Hz) **10**⁻¹⁵ **10⁻¹⁶ 10**⁻¹⁷ **10**⁻¹⁸ 10⁻³ 10⁻² 10⁻⁴ ا_د (A)

 $0.7 \times 100 \ \mu m^2 \ NPN, R_s = 100 \Omega$

$$S_{I_C} = KFC \cdot I_C^{AFC}$$
$$AFC = 3.05 \sim 3.58$$

no physical explanation for such high current dependence:

SPURIOUS?

Effect of interfacial oxide on S_{Vr}

 $0.7x100 \ \mu m^2 \ NPN, \ R_s = 100 \Omega$



$$S_{V_r} = S_{V_{r_e}} + S_{V_{r_b}}$$

$$S_{V_r} \approx S_{V_{r_e}}$$
$$= I_E^2 \cdot S_{r_e}$$

Effect of internal resistance in collector-emitter measurement

 $0.7x100 \ \mu m^2$ NPN, thickest IFO



Tunneling fluctuation through interfacial oxide



Interfacial oxide thickness

Relative	Emitter area	interfacial oxide thickness (Å) from			
IFO thickness	(µm²)	minority carrier		majority carrier	
		fluctuation (S _{IBT})		fluctuation (S _{Vre})	
		PNP	NPN	NPN	
	0.7x100	14.50		4.08	
thickest	0.7x10	16.90			
	0.7x2.8	14.50			
	0.7x0.7	11.00			
medium	0.7x100	4.13	11.30	2.26	
	0.7x0.7	8.78			
thinnest	0.7x100		2.70		
	0.7x0.7		2.81		

Inconsistency:

uncertainty in loss tangent, mass and potential barrier of the carriers at oxide interface.

$$V_h = 0.363V$$
 $V_e = 0.097V$
 $m_h^* = 0.81m_o$ $m_e^* = 1.08m_o$

 $\tan \delta$ obtained from Kleinpenning et. al, IEEE Trans. on Elec. Dev., vol. 42, 1995.

 V_h as high as 1.8V and V_e as high 1 V found in literature. tan δ unique for each sample.

Outline

- Introduction:
 - Limitations in existing noise models.
 - Importance and motivation of research.

• Noise in polysilicon emitter bipolar transistors:

- Experimental setup.
- S_{IB} modeling:
 - noise mechanisms, effect of bias, geometry and IFO.
- S_{IC} modeling:
 - noise mechanisms, effect of bias and IFO.
- S_{vr} modeling:
 - Collector-emitter measurement setup, effect of bias and IFO.

• Computer codes.

- Noise in SiGe heterojunction bipolar transistors:
 - Dominant noise source.
 - Effect of selective collector implant.
 - Effect of higher extrinsic base implant.
 - Effect of SiGe epi-SiGe poly interface.
 - Effect of emitter-poly overlap.
 - Physical origin and modeling of S_{IB.}
- Conclusion

Experimental and Simulated data



Computer source code

- Existing BERKELEY SPICE source code has been modified.
 - Source code written at Texas Instruments Inc. by Douglas Weiser.
 - S_{I_C} and S_{V_r} have been added to the existing noise model in addition to S_{I_R} .
 - An area scaling factor has been added to the equations to make the noise models scalable.

The modified BERKELEY SPICE source code is available to the SRC (Semiconductor Research Corporation) member companies (TI, Intel, IBM, Motorola, National Semiconductor Corporation, AMD, etc.)

Outline

- Introduction:
 - Limitations in existing noise models.
 - Importance and motivation of research.
- Noise in polysilicon emitter bipolar transistors:
 - Experimental setup.
 - S_{IB} modeling:
 - noise mechanisms, effect of bias, geometry and IFO.
 - S_{IC} modeling:
 - noise mechanisms, effect of bias and IFO.
 - S_{vr} modeling:
 - Collector-emitter measurement setup, effect of bias and IFO.
 - Computer codes.

Noise in SiGe heterojunction bipolar transistors:

Dominant noise source.

- Effect of selective collector implant.
- Effect of higher extrinsic base implant.
- Effect of SiGe epi-SiGe poly interface.
- Effect of emitter-poly overlap.
- Physical origin and modeling of S_{IB.}
- Conclusion

Device structure under investigation



Transistors described as x-y-z; e.g. SIC:25-10-25.

Dominant noise source



- Calculated S_{VC}/S_{VB} with S_{IB} contribution dominant closely matches experimental S_{VC}/S_{VB}; S_{IB} contribution dominant.
- I_B increases r_n decreases coherence increases.

UTA Noise and Reliability Laboratory

Outline

- Introduction:
 - Limitations in existing noise models.
 - Importance and motivation of research.
- Noise in polysilicon emitter bipolar transistors:
 - Experimental setup.
 - S_{IB} modeling:
 - noise mechanisms, effect of bias, geometry and IFO.
 - S_{IC} modeling:
 - noise mechanisms, effect of bias and IFO.
 - S_{vr} modeling:
 - Collector-emitter measurement setup, effect of bias and IFO.
 - Computer codes.

Noise in SiGe heterojunction bipolar transistors:

- Dominant noise source.
- Effect of selective collector implant.
- Effect of higher extrinsic base implant.
- Effect of SiGe epi-SiGe poly interface.
- Effect of emitter-poly overlap.
- Physical origin and modeling of S_{IB.}
- Conclusion



Effect of selectively implanted collector



SIC retards Kirk-effect

higher β for wider range of bias.

No degradation in noise.

Outline

- Introduction:
 - Limitations in existing noise models.
 - Importance and motivation of research.
- Noise in polysilicon emitter bipolar transistors:
 - Experimental setup.
 - S_{IB} modeling:
 - noise mechanisms, effect of bias, geometry and IFO.
 - S_{IC} modeling:
 - noise mechanisms, effect of bias and IFO.
 - S_{vr} modeling:
 - Collector-emitter measurement setup, effect of bias and IFO.
 - Computer codes.

Noise in SiGe heterojunction bipolar transistors:

- Dominant noise source.
- Effect of selective collector implant.
- Effect of higher extrinsic base implant.
- Effect of SiGe epi-SiGe poly interface.
- Effect of emitter-poly overlap.
- Physical origin and modeling of S_{IB.}
- Conclusion

Higher extrinsic base implant (HEBI)



Effect of higher extrinsic base implant



- Higher gain for higher extrinsic base implant is possibly due to relative changes in Ge profile.
- No degradation in noise.

Outline

- Introduction:
 - Limitations in existing noise models.
 - Importance and motivation of research.
- Noise in polysilicon emitter bipolar transistors:
 - Experimental setup.
 - S_{IB} modeling:
 - noise mechanisms, effect of bias, geometry and IFO.
 - S_{IC} modeling:
 - noise mechanisms, effect of bias and IFO.
 - S_{vr} modeling:
 - Collector-emitter measurement setup, effect of bias and IFO.
 - Computer codes.

Noise in SiGe heterojunction bipolar transistors:

- Dominant noise source.
- Effect of selective collector implant.
- Effect of higher extrinsic base implant.
- Effect of SiGe epi-SiGe poly interface.
- Effect of emitter-poly overlap.
- Physical origin and modeling of S_{IB.}
- Conclusion

SiGe epi-SiGe poly interface



Effect of SiGe epi-SiGe poly interface



- No significant impact on DC characteristics.
- No degradation in noise; boron implantation in extrinsic base passivates the interface-defects.

Outline

- Introduction:
 - Limitations in existing noise models.
 - Importance and motivation of research.
- Noise in polysilicon emitter bipolar transistors:
 - Experimental setup.
 - S_{IB} modeling:
 - noise mechanisms, effect of bias, geometry and IFO.
 - S_{IC} modeling:
 - noise mechanisms, effect of bias and IFO.
 - S_{vr} modeling:
 - Collector-emitter measurement setup, effect of bias and IFO.
 - Computer codes.

Noise in SiGe heterojunction bipolar transistors:

- Dominant noise source.
- Effect of selective collector implant.
- Effect of higher extrinsic base implant.
- Effect of SiGe epi-SiGe poly interface.
- Effect of emitter-poly overlap.
- Physical origin and modeling of S_{IB.}
- Conclusion

Effect of emitter-poly overlap



- Significant g-r noise for smaller emitter-poly overlap.
- g-r noise diminished at higher currents in comparison to increased 1/f noise.

Effect of emitter-poly overlap (cont.)



- Higher non-ideal base current for smaller emitter-poly overlap.
- S_{IB} deviates from ~I_B² dependence for smaller emitter-poly overlap.

Outline

- Introduction:
 - Limitations in existing noise models.
 - Importance and motivation of research.
- Noise in polysilicon emitter bipolar transistors:
 - Experimental setup.
 - S_{IB} modeling:
 - noise mechanisms, effect of bias, geometry and IFO.
 - S_{IC} modeling:
 - noise mechanisms, effect of bias and IFO.
 - S_{vr} modeling:
 - Collector-emitter measurement setup, effect of bias and IFO.
 - Computer codes.

Noise in SiGe heterojunction bipolar transistors:

- Dominant noise source.
- Effect of selective collector implant.
- Effect of higher extrinsic base implant.
- Effect of SiGe epi-SiGe poly interface.
- Effect of emitter-poly overlap.
- Physical origin and modeling of S_{IB.}
- Conclusion

Physical origin of S_{IB}



- All except smaller emitter-poly overlap $\eta_r \le 1.6$, AF ≈ 2 .
- Smaller emitter-poly overlap $\eta_r > 3$, AF ≈ 1 .

UTA Noise and Reliability Laboratory

$$AF \approx 2 \qquad S_{I_B} = KF_1 \cdot I_B^2 \qquad KF_1 = \sum_{i=1}^{N_1} I_B^2 \frac{\tau_i}{1 + (2\pi f \tau_i)^2}$$
$$N_1 : \text{Total number of} \\ \text{traps in emitter-} \\ \text{base junction.} \qquad \tau_i : \text{Characteristics time} \\ \text{constant of ith trap.}$$

Noise from Surface recombination current

S_{IB} model for smaller emitter-poly overlap

$$KF_{2} = \frac{q^{4}N_{2}\lambda}{KTAC_{sc}^{2}f}$$

$$N_{2}$$
: Oxide slow state volume density.

$$A : \text{Area of surface region.}$$

$$C_{sc} : \text{Surface capacitance per unit area.}$$

Separation of S_{IB} components

Outline

- Introduction:
 - Limitations in existing noise models.
 - Importance and motivation of research.
- Noise in polysilicon emitter bipolar transistors:
 - Experimental setup.
 - S_{IB} modeling:
 - noise mechanisms, effect of bias, geometry and IFO.
 - S_{IC} modeling:
 - noise mechanisms, effect of bias and IFO.
 - S_{Vr} modeling:
 - Collector-emitter measurement setup, effect of bias and IFO.
 - Computer codes.
- Noise in SiGe heterojunction bipolar transistors:
 - Dominant noise source.
 - Effect of selective collector implant.
 - Effect of higher extrinsic base implant.
 - Effect of SiGe epi-SiGe poly interface.
 - Effect of emitter-poly overlap.
 - Physical origin and modeling of S_{IB.}

Conclusion

Polysilicon emitter bipolar transistors:

- The base current fluctuations dominate at relatively high external base resistance values.
- Collector current fluctuations contribute when the external base resistance becomes comparable to or less than the input resistance.
- Fluctuations caused by the internal emitter resistance take over for high currents with small base resistance.
- From the dependence of noise magnitude on the geometry and temperature, fluctuations in the non-ideal base current was neglected.

Conclusion (cont.)

- S_{IB} originates from diffusion fluctuations of minority carriers in poly and monosilicon emitter, and tunneling fluctuations of minority carriers at IFO; S_{IC} from diffusion and number fluctuations of minority carriers in base, and S_{Vre} from tunneling fluctuations of majority carrier at IFO.
- Diffusion fluctuations dominate over the tunneling fluctuations for larger devices; tunneling fluctuations dominate over diffusion fluctuations for the smaller ones.
- IFO increases the current gain significantly in NPN; both tunneling and diffusion fluctuations contribute.
- No significant improvement with increasing IFO thickness in PNP; diffusion fluctuations dominant.

SiGe heterojunction bipolar transistors:

- Selectively implanted collector causes higher current gain for wider range of bias; no noise degradation.
- No significant effect of SiGe epi-SiGe poly interface and higher extrinsic base implant.
- Severe impact of smaller emitter-poly overlap:
 - increases non-ideality of the base current; trap assisted tunneling current due to parasitic BJT.
 - g-r noise at lower bias currents.
 - At higher bias currents, fluctuations from trap assisted tunneling current contribute.
- For all transistors except smaller emitter poly overlap, noise originates from intrinsic E-B junction.

Acknowledgements

Supervising Professor:

- Zeynep Celik-Butler
- Semiconductor Research Corporation:
- Texas Instruments Inc.
- National Semiconductor Corporation
- Texas Higher Education Board, Advanced Technology Prog.
- UTA Noise & Microsensor Group:
- Bigang Min, Siva P. Devireddy, Shadi Dayeh, Enhai Zhao